Sup*IR*Buck™

USER GUIDE FOR IR3859 EVALUATION BOARD

DESCRIPTION

The IR3859 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 4mmx5mm Power QFN package.

Key features offered by the IR3859 include programmable soft-start ramp, precision 0.7V reference voltage, Power Good, thermal protection, over voltage protection, programmable switching frequency, synchronization to external clock, Sequence input, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3859 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3859 is available in the IR3859 data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{cc}=+5V (5.5V Max)
- V_{out} = +1.8V @ 0- 9A
- F_s=600kHz
- L= 0.68uH
- C_{in}= 4x10uF (ceramic 1206) + 330uF (electrolytic)
- C_{out}= 6x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 9A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3859 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

If single 12V application is required connect R7 (zero Ohm resistor) which enables the on board bias regulator (see schematic). In this case there is no need of external Vcc supply.

The output can track a sequencing input at the start-up. *For sequencing application, R16 should be removed and the external sequencing source should be applied between Seq. and Agnd.* The value of R14 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. *For proper operation of IR3859, the voltage at Seq. pin should not exceed Vcc.*

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
Enable	Enable
Seq.	Sequence Input
PGood	Power Good Signal
SYNC	External Synchronization Clock

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3859 SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3859. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

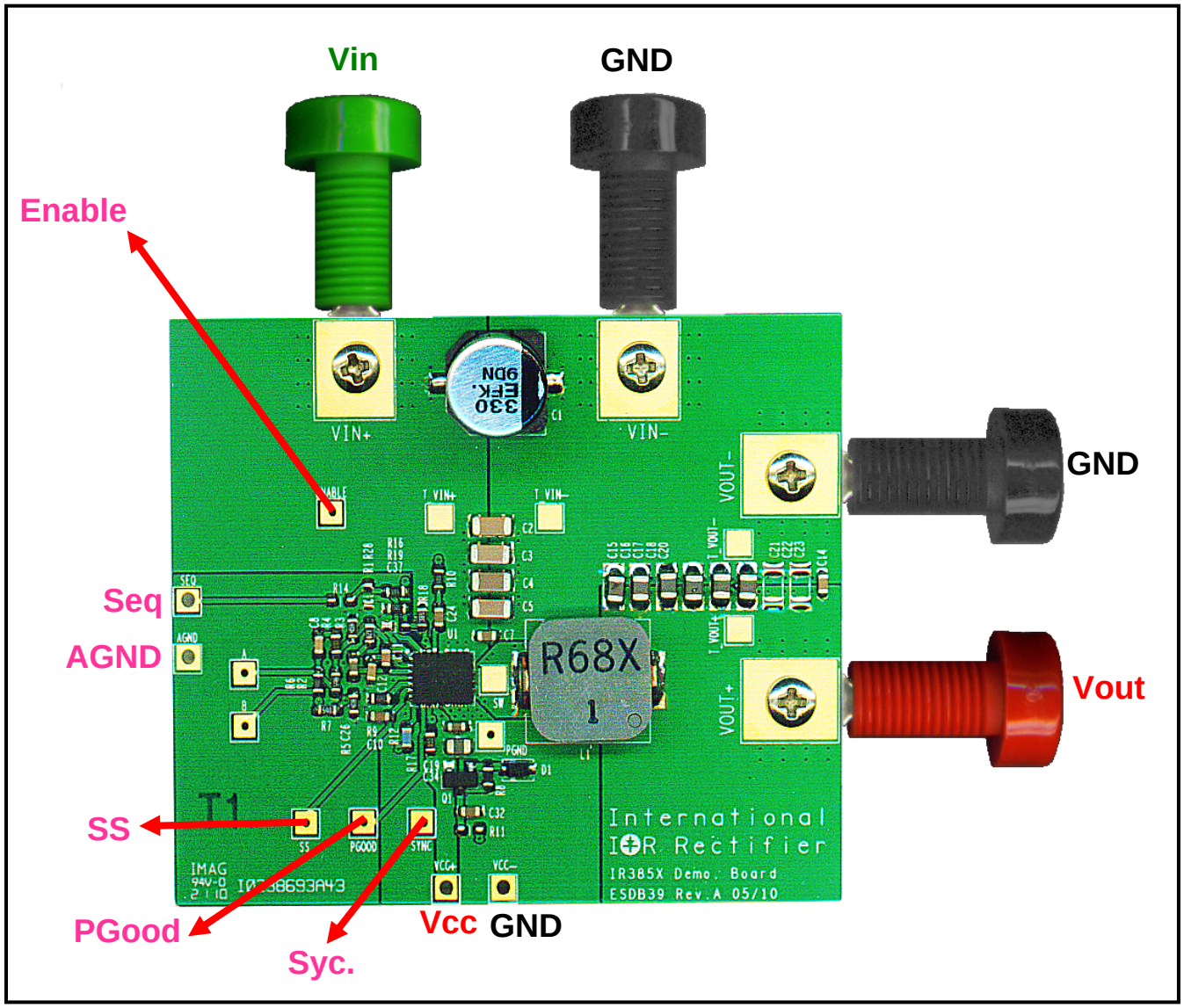


Fig. 1: Connection diagram of IR385x evaluation boards

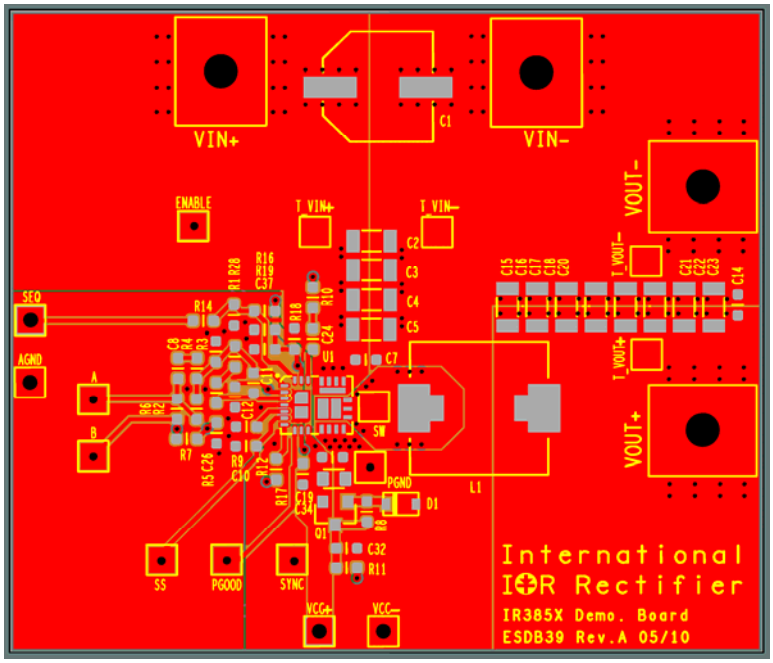


Fig. 2: Board layout, top overlay

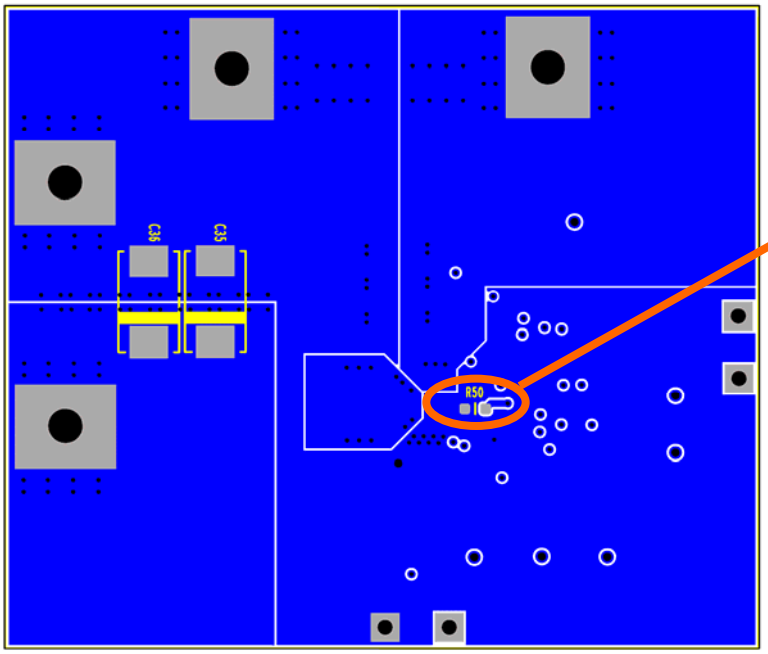


Fig. 3: Board layout, bottom overlay (rear view)

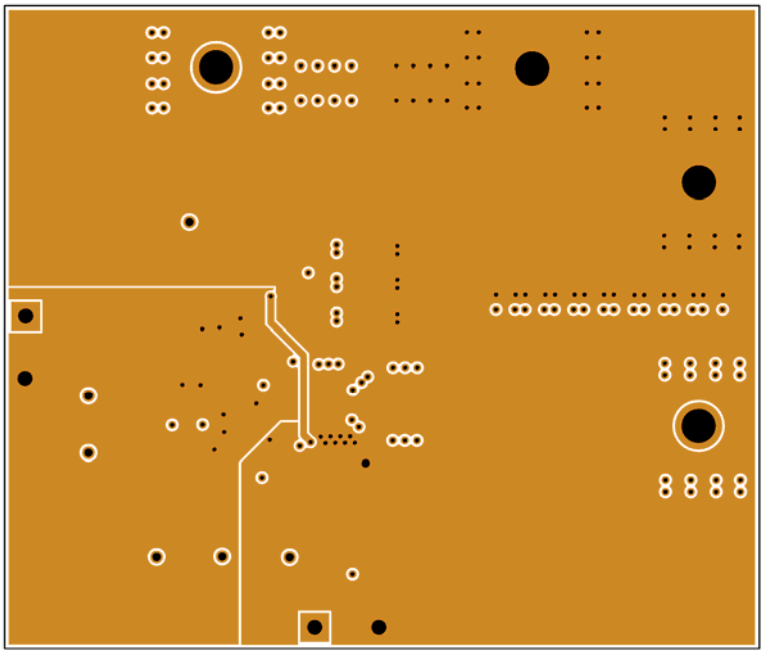


Fig. 4: Board layout, mid-layer I.

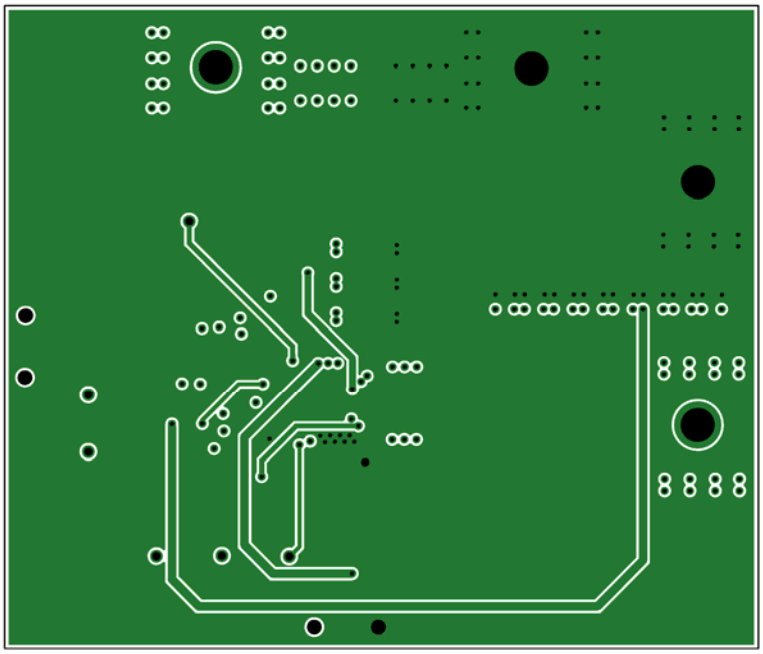


Fig. 5: Board layout, mid-layer II.

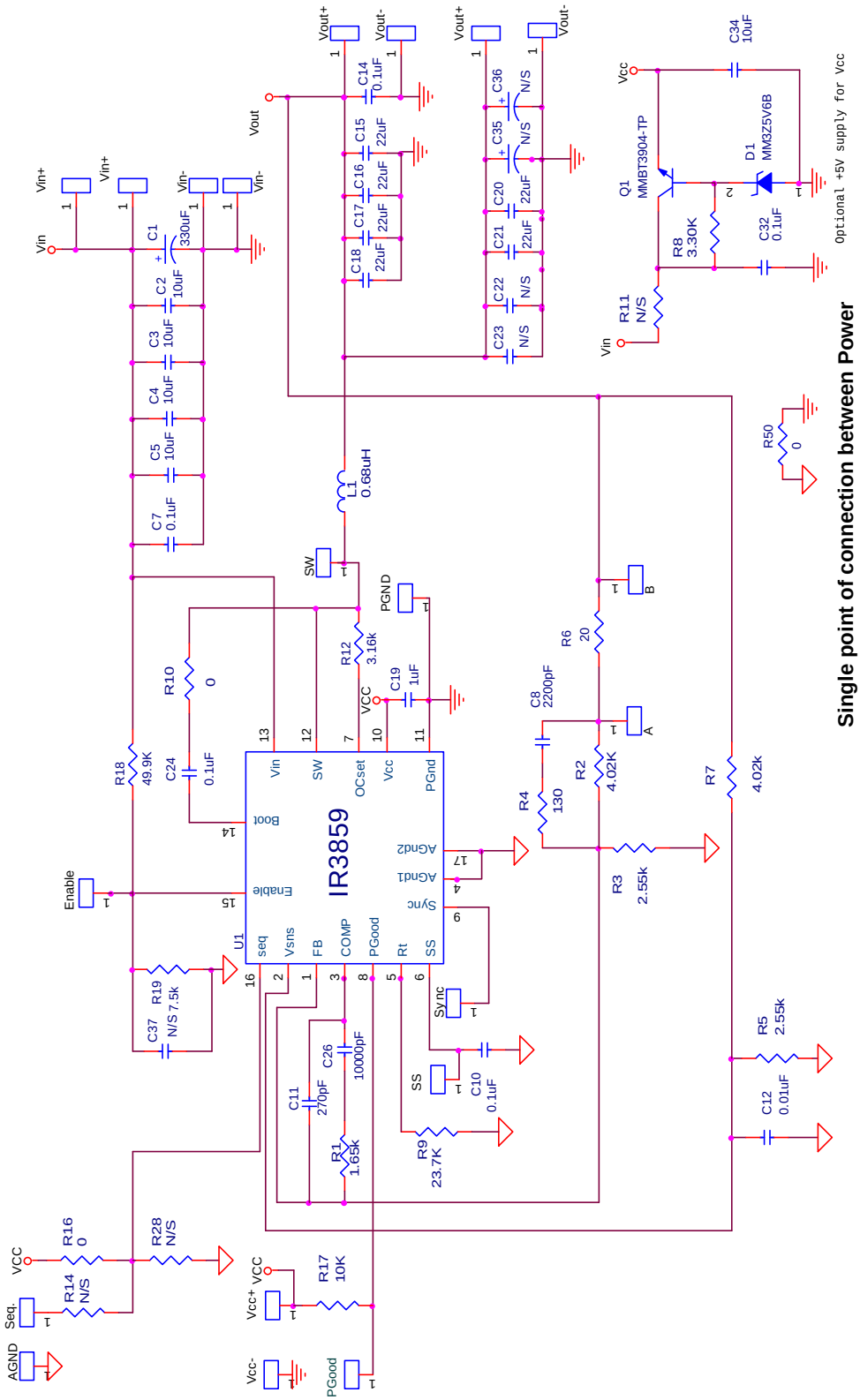


Fig. 6: Schematic of the IR3859 evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
2	4	C5 C4 C3 C2	10uF	1206, 25V, X5R, 20%	Murata	GRM31CR61E106MA12L
3	1	C34	10uF	0805, 10V, X5R, 20%	TDK	C2012X5R1A106KB
4	1	C19	1uF	0603, 16V, X7R, 10%	TDK	C1608X7R1C105K
5	1	C12	0.01uF	0603, 50V, X7R, 10%	TDK	C1608X7R1H103K
6	5	C7 C10 C14 C24 C32	0.1uF	0603, 25V, X7R, 10%	TDK	C1608X7R1H104KB
7	1	C8	2200pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H222JA01D
8	1	C11	270pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H271JA01D
9	6	C15 C16 C17 C18 C20 C21	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
10	1	C26	10000pF	0603, 25V, X7R, 10%	TDK	C1608X7R1E103K
11	1	D1	MM3Z5V6B	MM3Z5V6B,Zener, 5.6V	Fairchild	MM3Z5V6B
12	1	L1	0.68uH	11.7x10x4mm, 20%, 1.5mOhm	Panasonic	ETQP4LR68XFC
13	1	Q1	MMBT3904/SOT	NPN, 40V, 200mA, SOT-23	Fairchild	MMBT3904/SOT
14	1	R8	3.3k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3301
15	1	R18	49.9k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4992
16	1	R4	130	Thick Film, 0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF1300V
17	1	R6	20	Thick Film, 0603,1/10 W,1%	Vishey/Dale	CRCW060320R0FKEA
18	1	R9	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
19	3	R16 R10 R50	0	Thick Film, 0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
20	1	R12	3.16k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX3161
21	2	R3 R5	2.55k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX2551
22	1	R17	10.0k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1002
23	1	R19	7.50k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX7501
24	1	R1	1.65k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1651
25	2	R2 R7	4.02k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4021
26	1	U1	IR3859	PQFN 4mmx5mm, 9A SupIRBuck	International Rectifier	IR3859MPbF

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0-9A, Room Temperature, No Air Flow

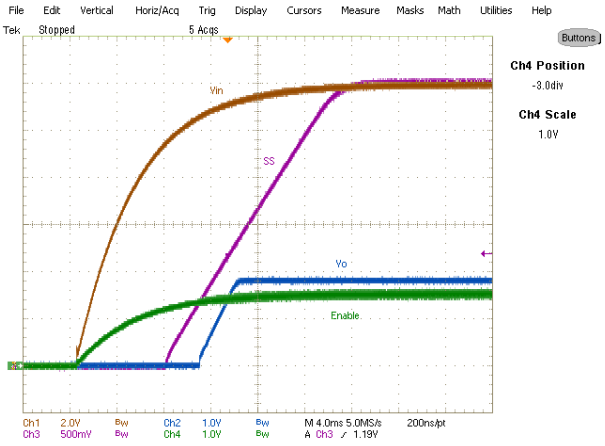


Fig. 7. Start up at 9A Load
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:Enable

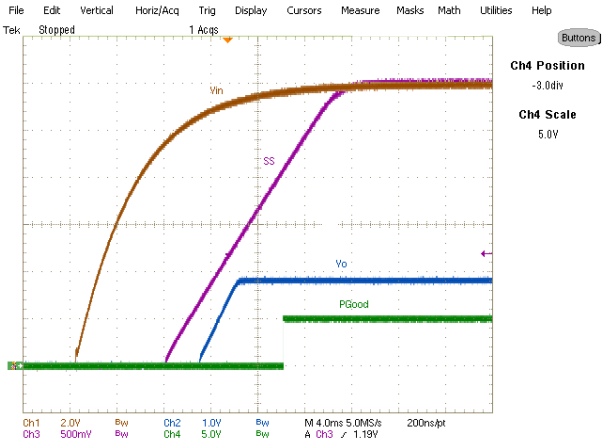


Fig. 8. Start up at 9A Load,
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:V_{PGood}

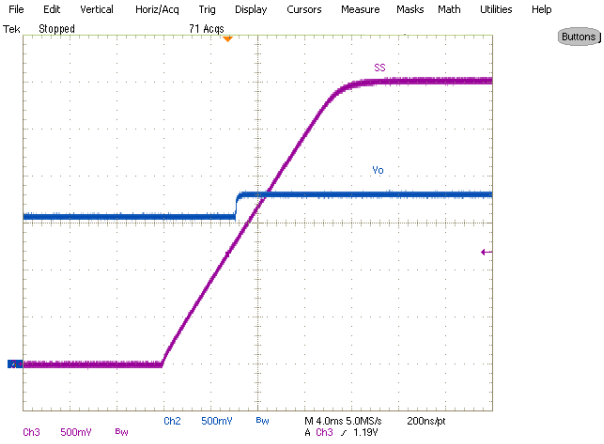


Fig. 9. Start up with 1.62V Pre Bias, 0A Load, Ch_2:V_o, Ch_3:V_{SS}

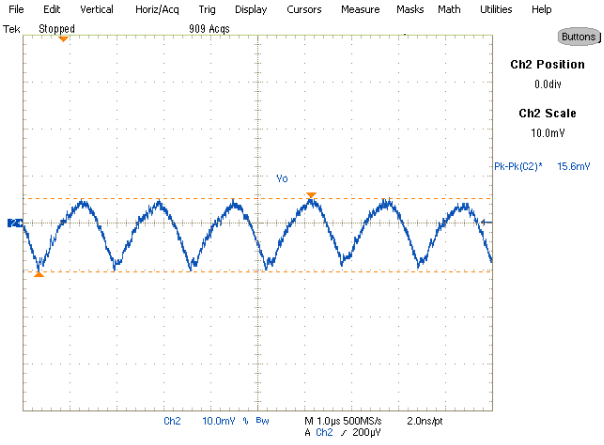


Fig. 10. Output Voltage Ripple, 9A load
Ch_2: V_o

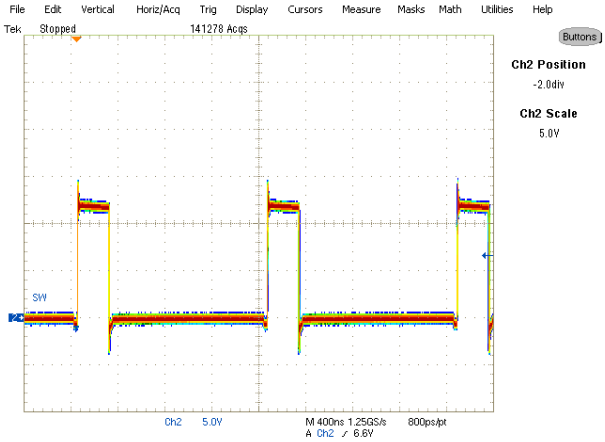


Fig. 11. Inductor node at 9A load
Ch_2:Switch Node

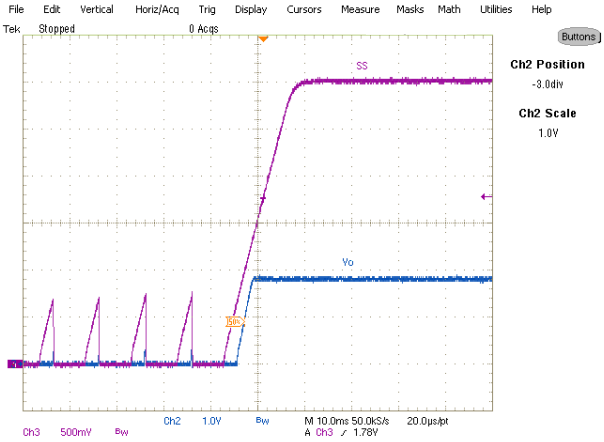


Fig. 12. Short (Hiccup) Recovery
Ch_2:V_o , Ch_3:V_{SS}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0-9A, Room Temperature, No Air Flow

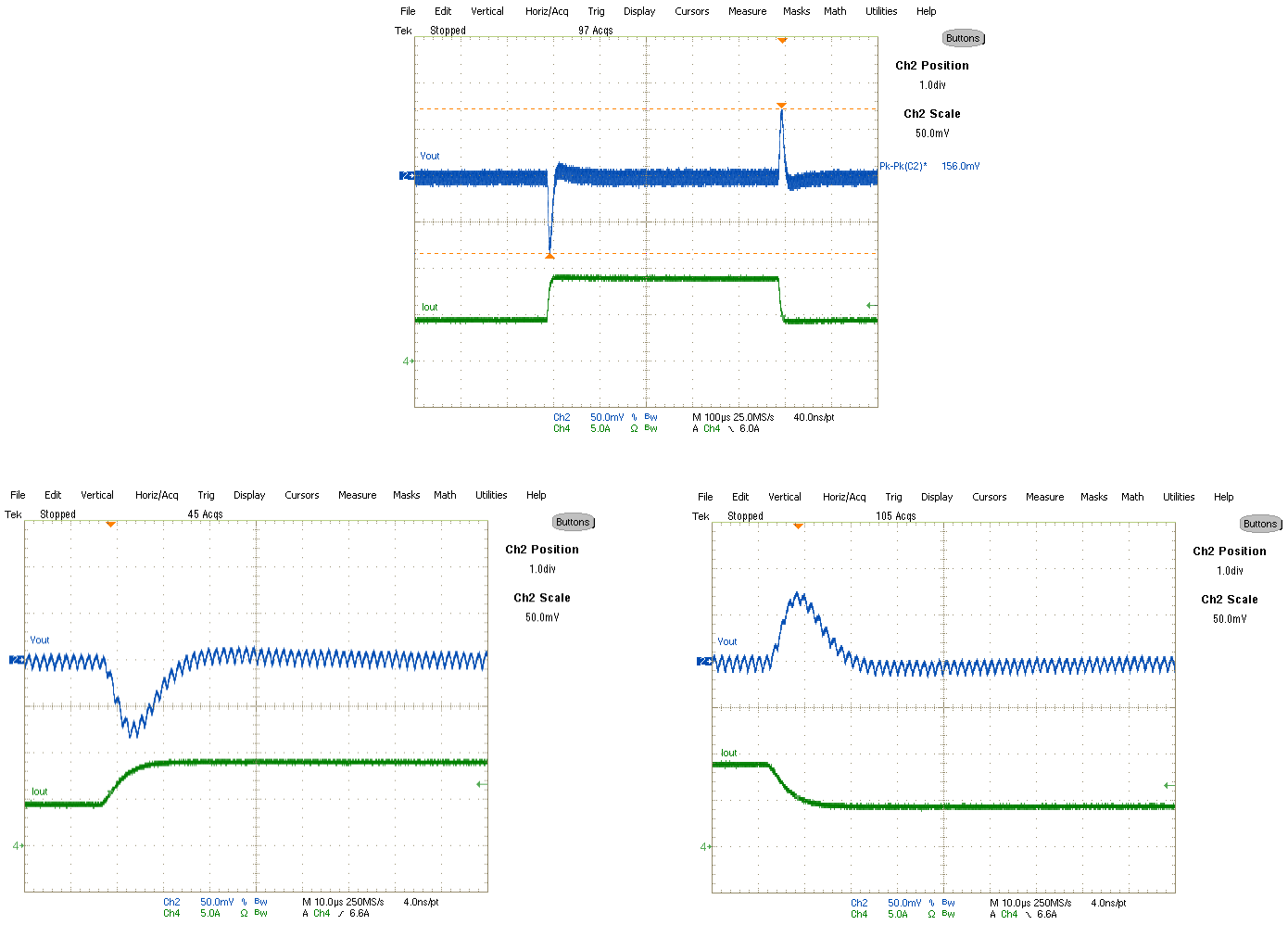


Fig. 13. Transient Response, 4.5A to 9A step 2.5A/µs
Ch_2:V_o, Ch_4:I_o

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=9A, Room Temperature, No Air Flow

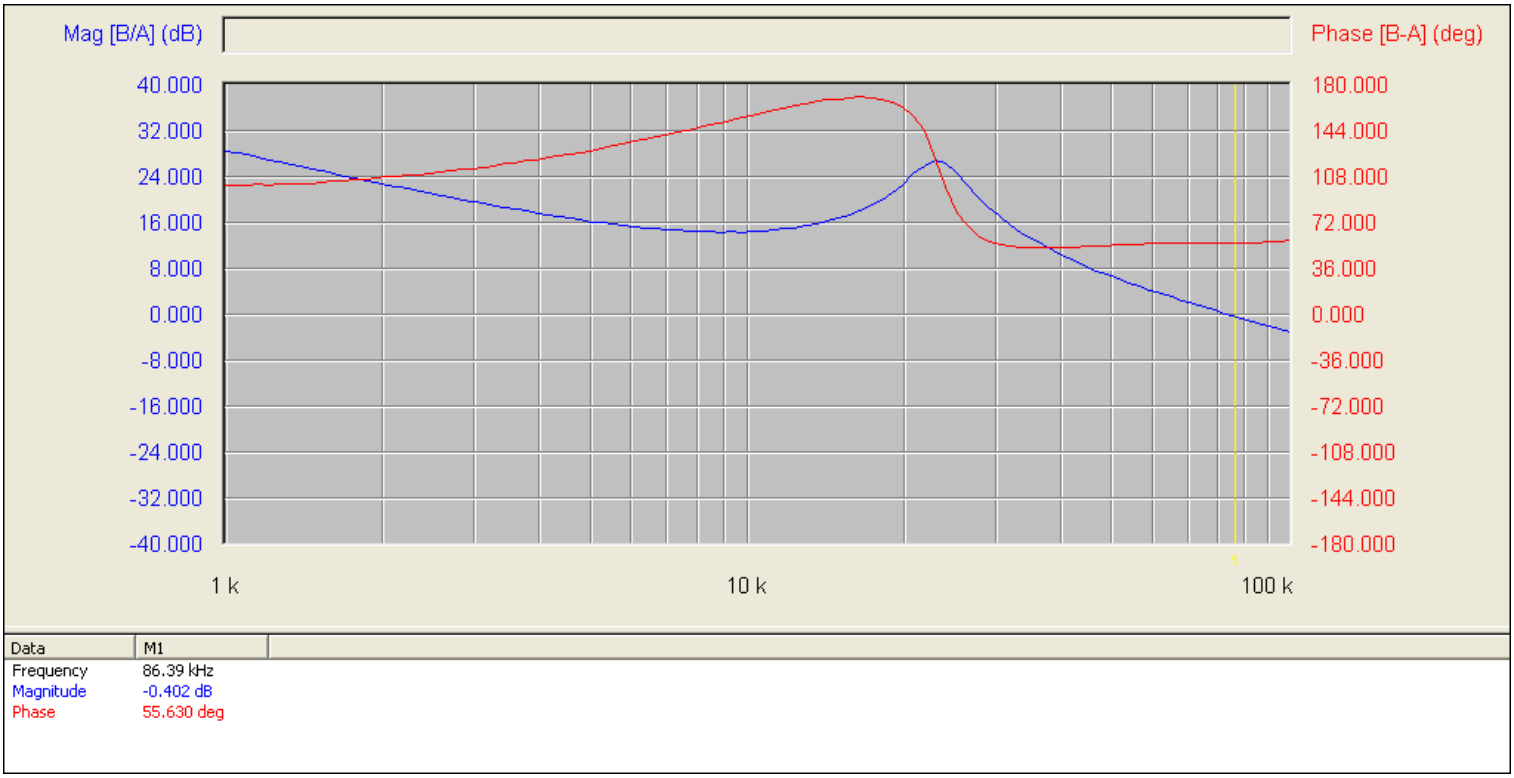


Fig. 14. Bode Plot at 9A load shows a bandwidth of 86.4kHz and phase margin of 55.6 degrees

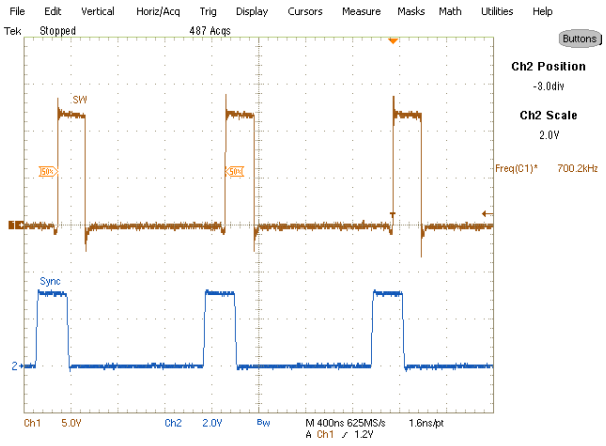


Fig. 15. Synchronization to External Clock
Ch_1:Switch node, Ch_2: Sync. Pin

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=1.8V, Io=0- 9A, Room Temperature, No Air Flow

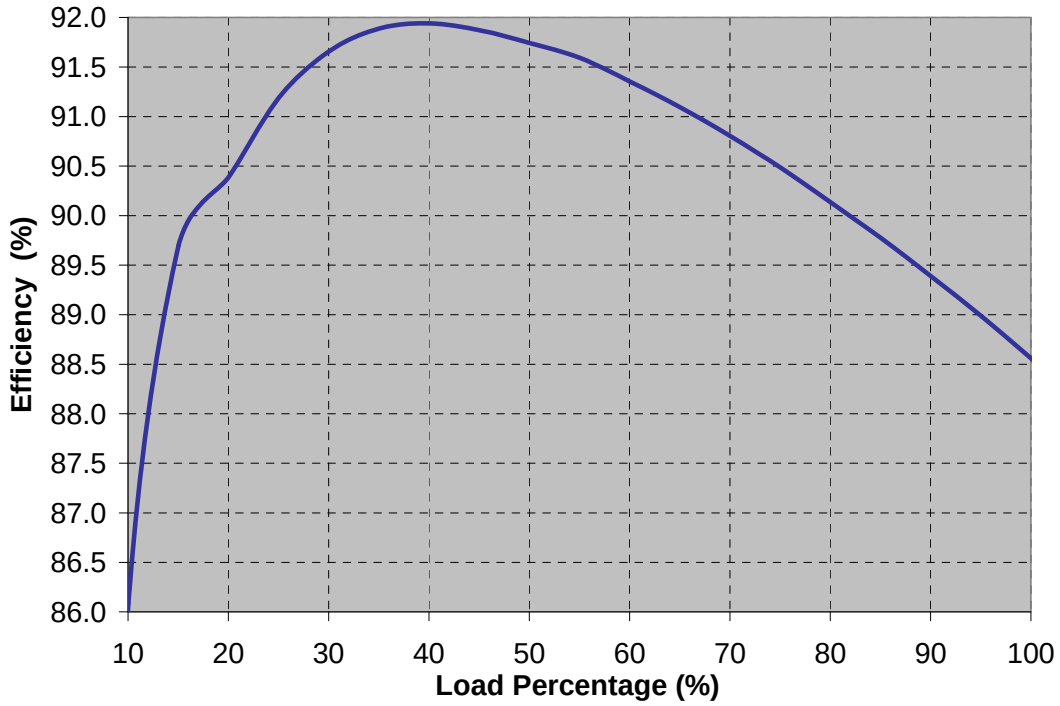


Fig.16: Efficiency versus load current

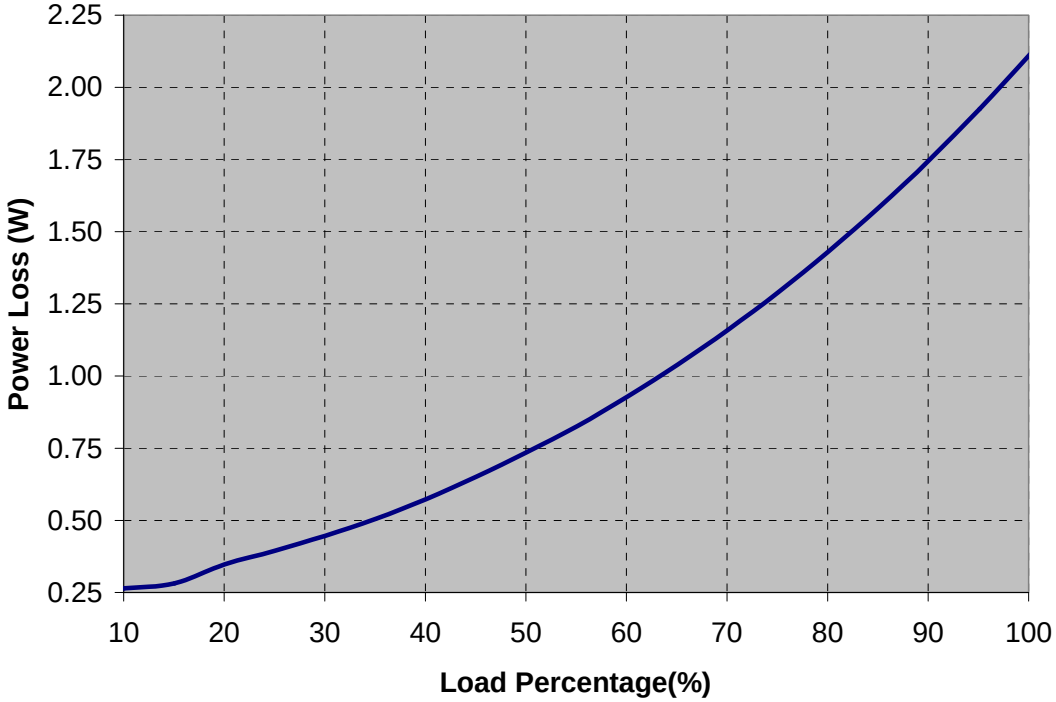


Fig.17: Power loss versus load current

THERMAL IMAGES
Vin=12V, Vo=1.8V, Io=9A, Room Temperature, No Air Flow

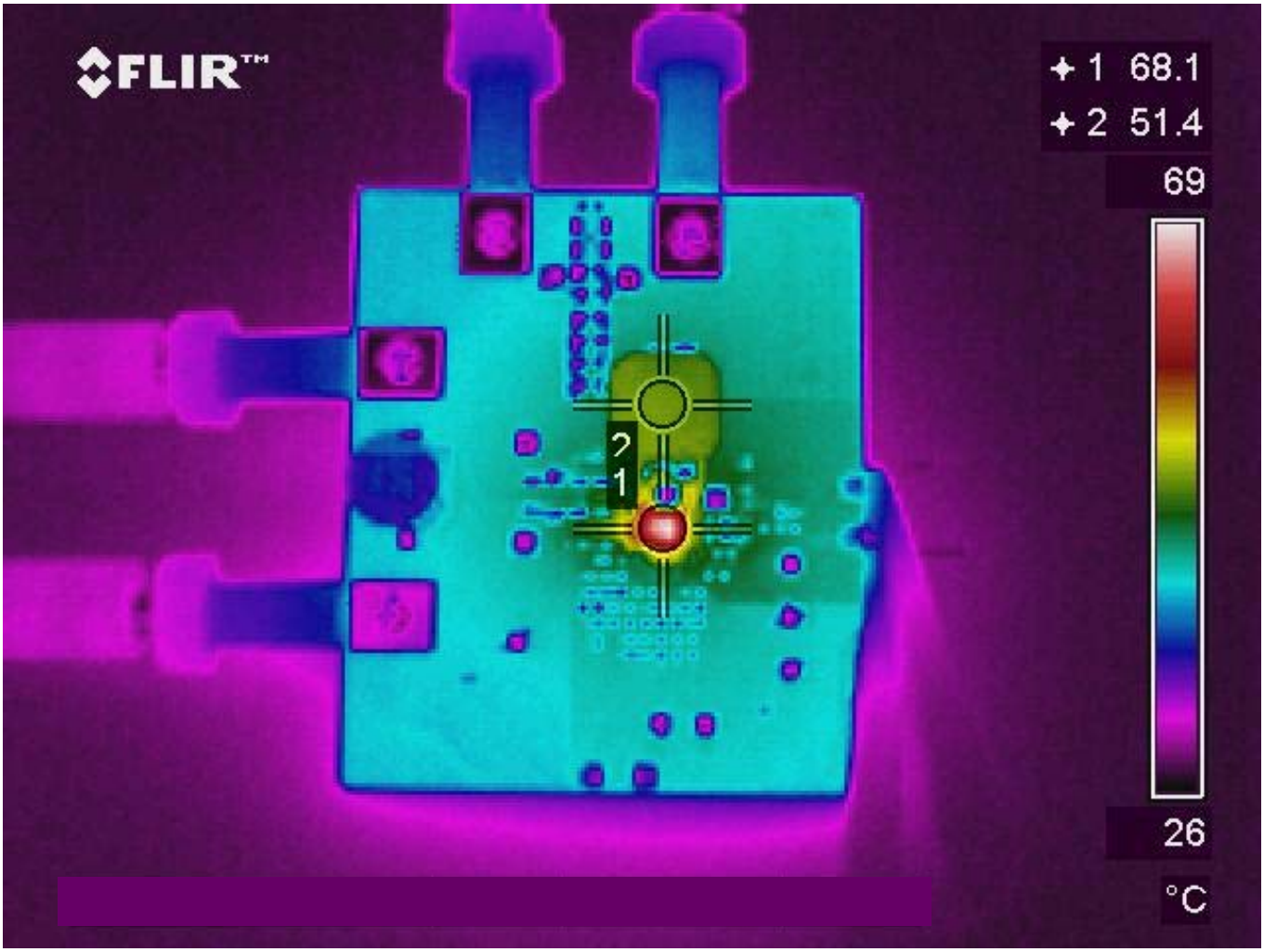


Fig. 18: Thermal Image at 9A load
Test points 1 and 2 are IR3859 and inductor, respectively.

Simultaneous Tracking at Power Up and Power Down
Vin=12V, Vo=1.8V, Io=9A, Room Temperature, No Air Flow

In order to run the IR3859 in the simultaneous tracking mode, the following steps should be taken:

- Remove R16 from the board.
- Set the value of R14 and R28 as R2 (4.02K) and R3 (2.55K), respectively.
- Connect the controlling input across SEQ and AGND test points on the board. This voltage should be at least 1.15 time greater than Vo. For the following test results a 0-3.3V source is applied to SEQ input.
- The controlling input should be applied after the SS pin is clamped to 3.0V.

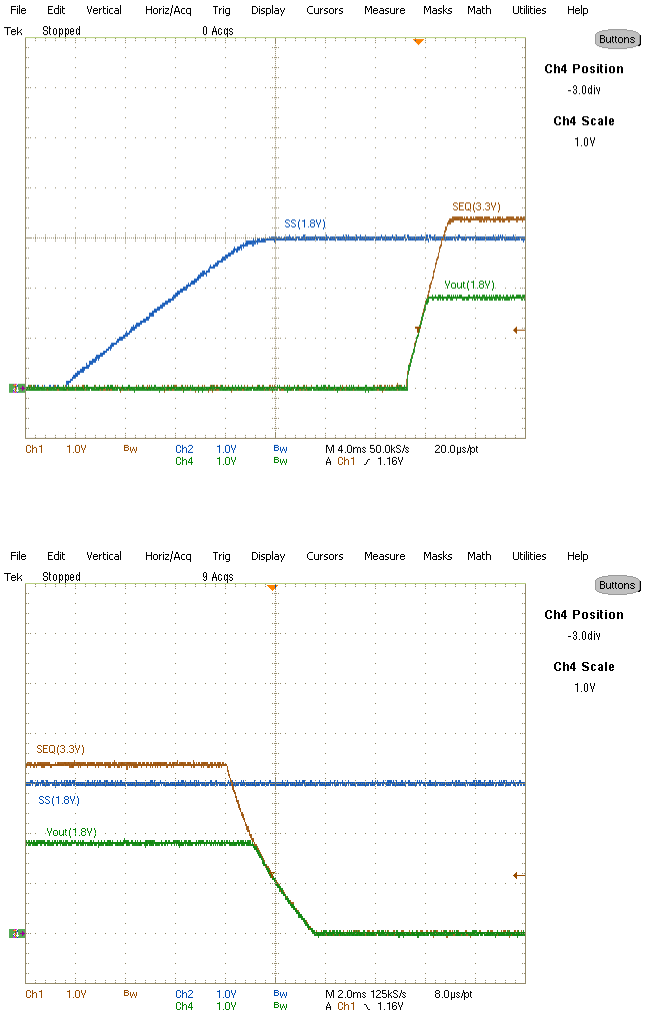
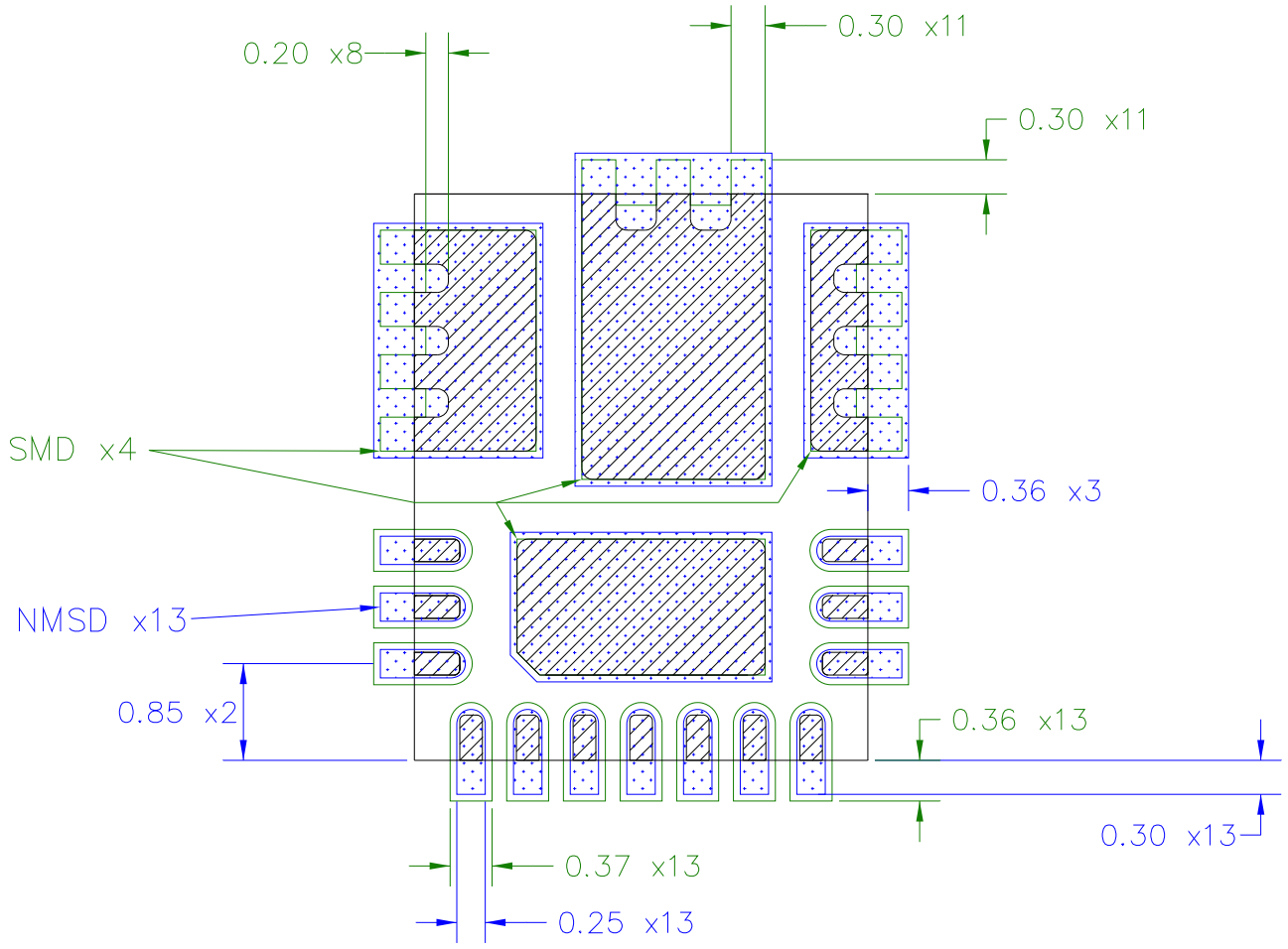


Fig. 19: Simultaneous Tracking a 3.3V input at power-up and shut-down
Ch1: SEQ (3.3V) Ch3:Vout (1.8V) Ch4: SS (1.8V)

PCB Metal and Components Placement



All Dimensions in mm

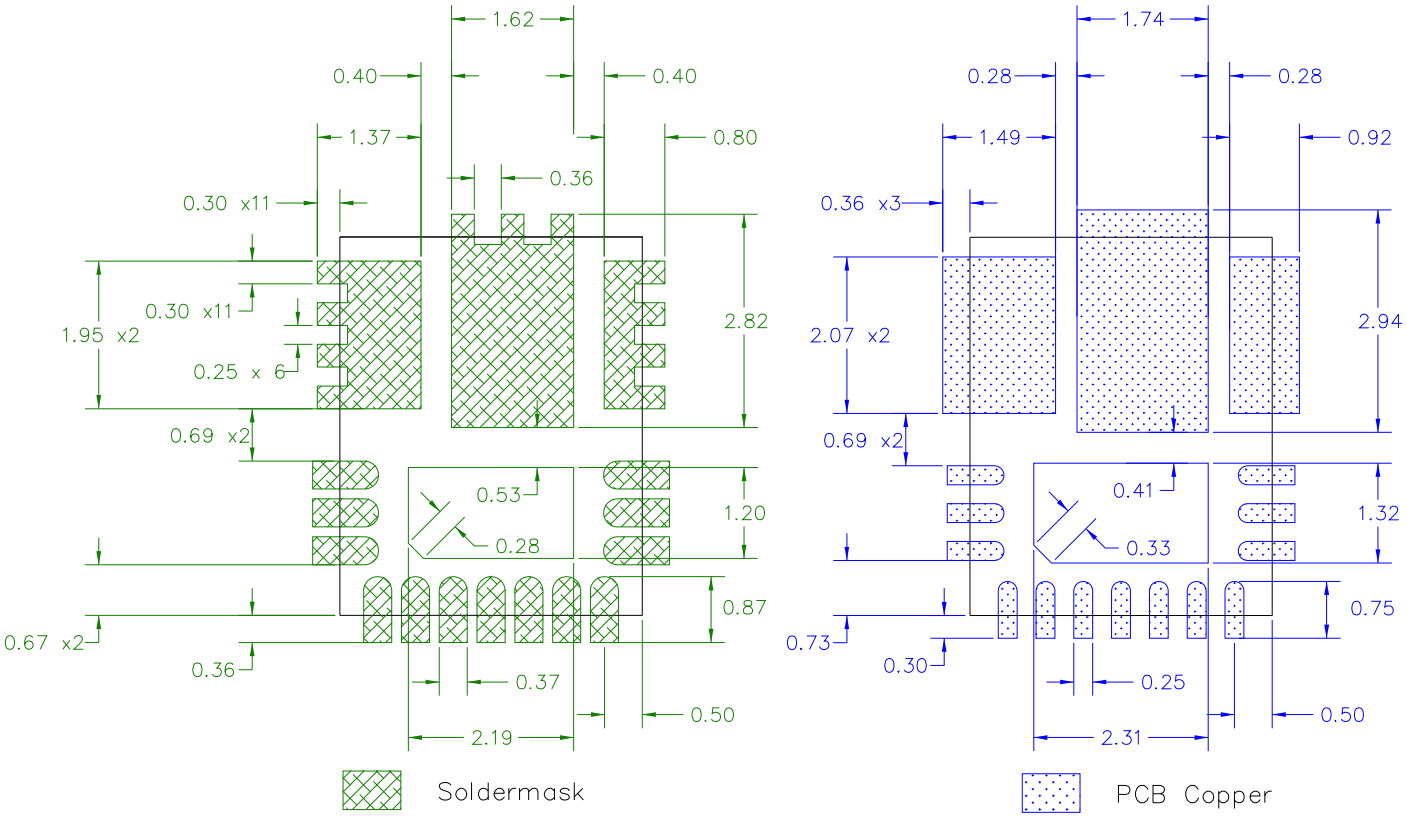
PCB Copper

Component

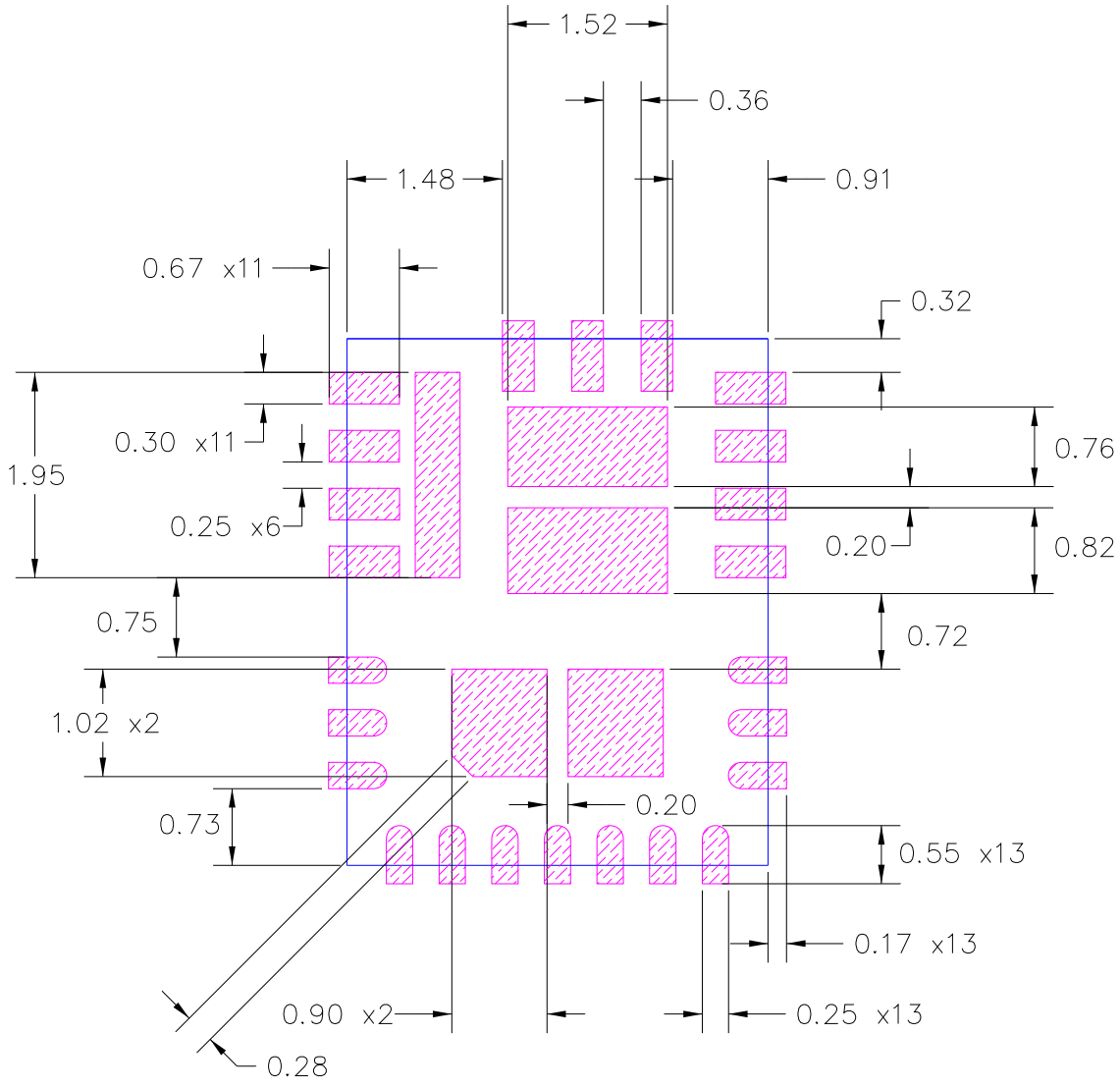
Soldermask

Solder Resist

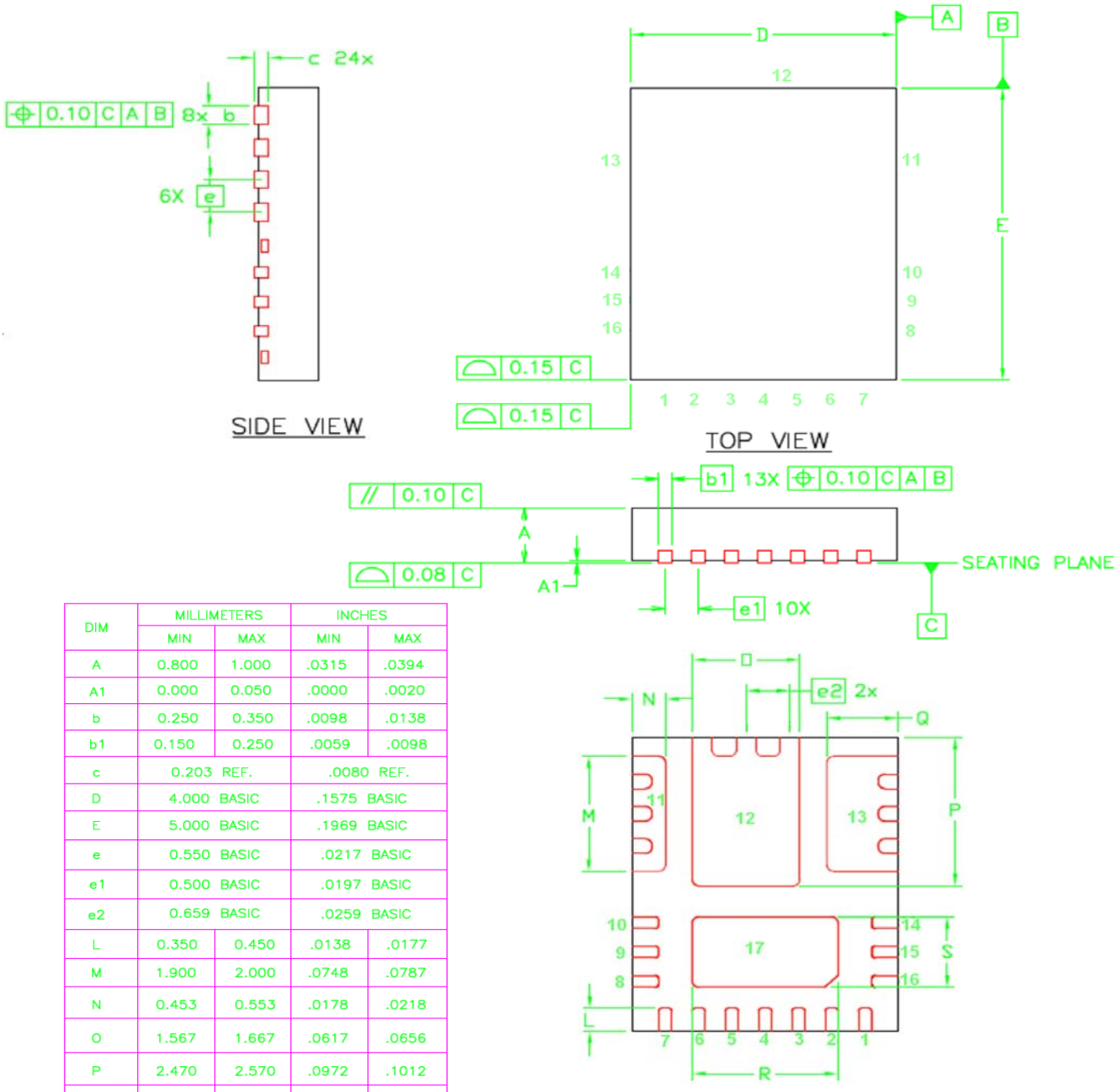
All Dimensions in mm



Stencil Design



Stencil Aperture
All Dimensions in mm



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.250	0.350	.0098	.0138
b1	0.150	0.250	.0059	.0098
c	0.203 REF.		.0080 REF.	
D	4.000 BASIC		.1575 BASIC	
E	5.000 BASIC		.1969 BASIC	
e	0.550 BASIC		.0217 BASIC	
e1	0.500 BASIC		.0197 BASIC	
e2	0.659 BASIC		.0259 BASIC	
L	0.350	0.450	.0138	.0177
M	1.900	2.000	.0748	.0787
N	0.453	0.553	.0178	.0218
O	1.567	1.667	.0617	.0656
P	2.470	2.570	.0972	.1012
Q	1.024	1.124	.0403	.0443
R	2.138	2.238	.0842	.0881
S	1.150	1.250	.0453	.0492

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